The foregoing amendments are made pursuant to a telephone interview between the undersigned and Examiner Tse on November 20, 2001.

Applicant requests approval of the amendments to FIGS. 1, 4 and 9 shown in the Request for Approval of Drawing Changes being filed concurrently herewith. These changes are basically being made to clarify that FIGS. 4 and 9 show in more detail one of the complex signal paths of the front end of FIG. 1. Corresponding amendments are also being made in the written description.

In the pending Office action, claim 10 was rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. The foregoing amendments to the written description and drawings clarify how they corresponds to claim 10. Specifically, the front end comprises elements 12, 14 and 18 in FIG. 1. The first tracking loop, which is represented by block 30 in FIG. 1, comprises blocks 66 and 70 in FIG. 4. The second tracking loop, which is also represented by block 30 in FIG. 1, comprises block 68 and 72 in FIG. 4. The third tracking loop, which is also represented by block 30 in FIG. 1, comprises blocks 76, 78 and 80 in FIG. 4.

Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

In view of the amendments made at this time and the foregoing remarks, reconsideration and allowance of this application are requested.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____

LeRoy T. Rahn
Reg. No. 20,356
626/795-9900

LTR/amb

VERSION TO SHOW CHANGES MADE

In the Specification:

Please amend the paragraph beginning on page 7, Line 24, to read as follows:

FIG. 4 is a [simplified, semi-schematic] more detailed block diagram of the architecture of [carrier recovery and baud loops of a dual mode QAM/VSB receiver in accordance with the invention] FIG. 1;

Please amend the paragraph beginning on page 7, Line 29, to read as follows:

FIG. 6 is a graphical representation of the [affects] effects of the low pass, high pass and equivalent bandpass filters of FIG. 5 on an input spectrum, where the [filter's] cutoff frequencies of the filters have an integer relationship to the sampling frequency;

Please amend the paragraph beginning on page 7, Line 33, to read as follows:

FIG. 7 is a simplified, semi-schematic block diagram of a baud loop as might be implemented in [a] the dual mode QAM/VSB receiver architecture [in accordance with the invention] of FIG. 1;

Please amend the paragraph beginning on page 8, Line 6, to read as follows:

FIG. 9 is a simplified, semi-schematic block diagram of a dual mode QAM/VSB receiver architecture, including the decision directed carrier phase tracking circuitry [in accordance with the invention] of FIG. 4;

Please amend the paragraph beginning on page 20, line 17, to read as follows:

In-phase (I) and quadrature phase (Q) baseband signals are then filtered by square-root Nyquist filters 22 which can accommodate roll-off factors of 11-18%. The outputs of the square-root Nyquist filters are subsequently directed by a complex digital mixer 58 to an adaptive equalization block 24 and are parallel-processed by a Nyquist-type prefilter 26 to provide an input signal to an acquisition/tracking loop circuit 30 which includes carrier recovery loop circuitry to support carrier frequency recovery and spectrum centering as well as baud recovery loop circuitry,

for symbol timing extraction, as will be described in greater detail below. A carrier frequency recovery control signal produced by circuit 30 is applied to an input of mixer 18. A spectrum centering control signal from circuit 30 is applied to an input of mixer 58. The baud recovery control signal from circuit 30 is applied to HB/VIB 20 to sample the signal from mixer 18.

Please amend the paragraph beginning on page 27, line 22, to read as follows:

Turning now to FIG. 4, there is depicted in detail, one of the complex signal paths of the front end architecture described in FIG. 1, illustrating the acquisition/tracking loops comprising circuit 30. [in simplified, semi-schematic block diagram form, an exemplary embodiment of a unitary carrier and recovery and symbol timing loop architecture, termed] This arrangement can be regarded as "unitary" in that both functions, frequency acquisition and tracking and symbol timing (also termed "baud recovery") are operable in response to the pilot (unsuppressed carrier) signal. In the embodiment of FIG. 4, an input IF spectrum is digitized by an analog-to-digital converter (A/D) and the resulting digital complex signal is directed to a complex mixer 50 where it is combined with a complex signal having a characteristic frequency fC equal to the carrier frequency. The resulting complex signal is processed by a highband filter and variable rate interpolator, represented as a single processing block in the embodiment of FIG. 4, and denoted HB/VID 52. In a manner to be described in greater detail below, symbol timing is performed by a baud loop coupled to provide symbol timing information to the variable rate interpolator (VID) portion of the HB/VID filter 52. Following interpolation, baseband IF signals are processed by a square root Nyquist filter which has a programmable roll off α of from about 11 to about 18%. The square root Nyquist filter 54 is further designed to have a particular cutoff frequency that has a specific relationship to the VSB pilot frequency fC, when the VSB spectrum centers at DC. In a manner to be described in greater detail below, this particular cutoff frequency is chosen to have this particular relationship in order that both carrier recovery and symbol timing recovery might be based on a VSB pilot frequency enhancement methodology.

Please amend the paragraph beginning on page 36, line 9, to read as follows:

Turning now to FIG. 9, there is depicted a simplified, semi-schematic block level diagram of one of the complex signal paths of the front end of FIG. 4 incorporated in a dual mode baseband architecture. [of the exemplary] A dual mode QAM/VSB receiver, [including] includes details of the construction and arrangement of adaptive equalizer 24 having decision directed VSB phase tracking and decision directed QAM frequency acquisition and phase tracking loops in accordance with the present invention. As illustrated in the embodiment of FIG. 9, the adaptive equalizer includes a feedforward (FFE) block 110 configured to receive symbol aligned complex signals centered in baseband. The FFE 110 is suitably constructed as either a 64-tap real FFE, for VSB applications, or a 16-tap complex FFE when used in connection with QAM modulated signals. Carrier phase alignment and/or carrier frequency/phase alignment is performed in a mixer 112 which receives signals from the FFE 110 and combines them with a timing reference signal developed by a timing reference circuit 114 such as a numerically controlled oscillator (NCO) a voltage controlled oscillator (VCO) or a direct digital frequency synthesizer (DDDFS). Timed signals are then provided to a slicer 116 operating in conjunction with a decision feedback (DFE) block 118 which, in combination, provide hard decision information on constellation states as well as error information relating to differences between actual signal trajectory relative to an ideal signal trajectory.

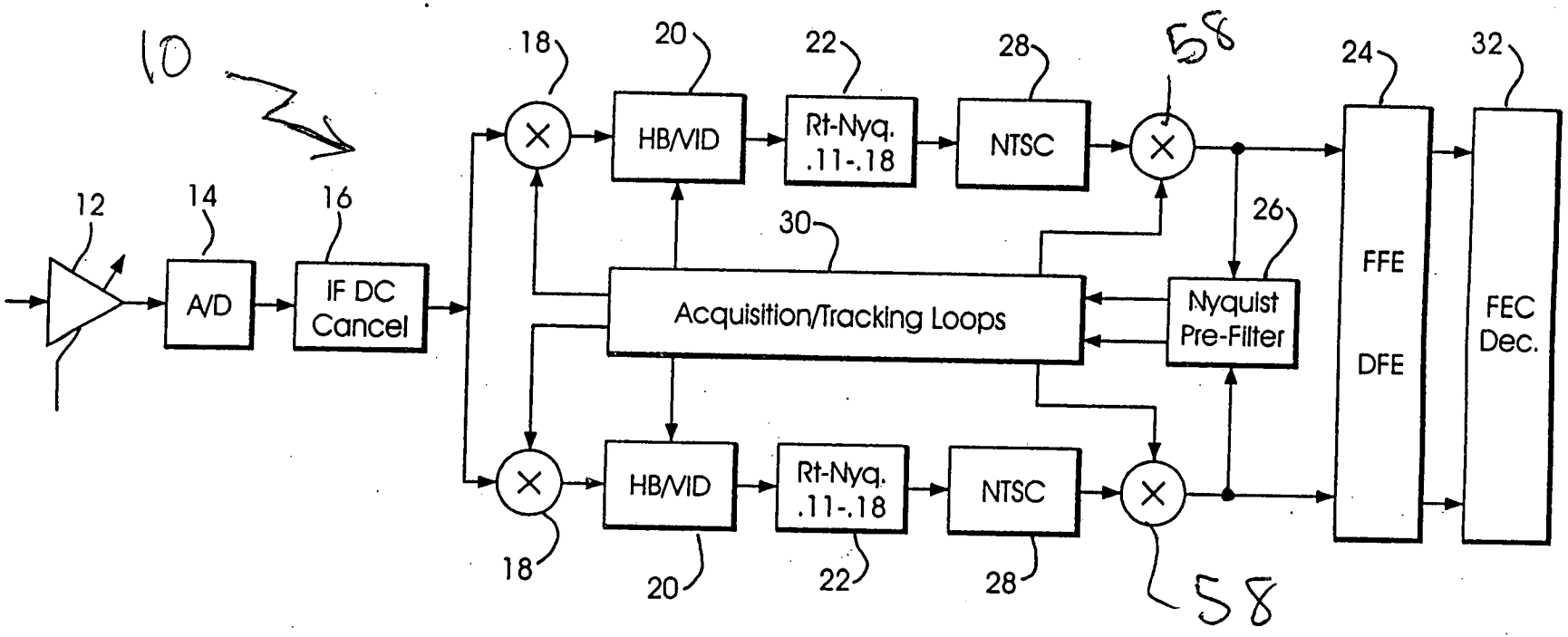
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FIG. 1

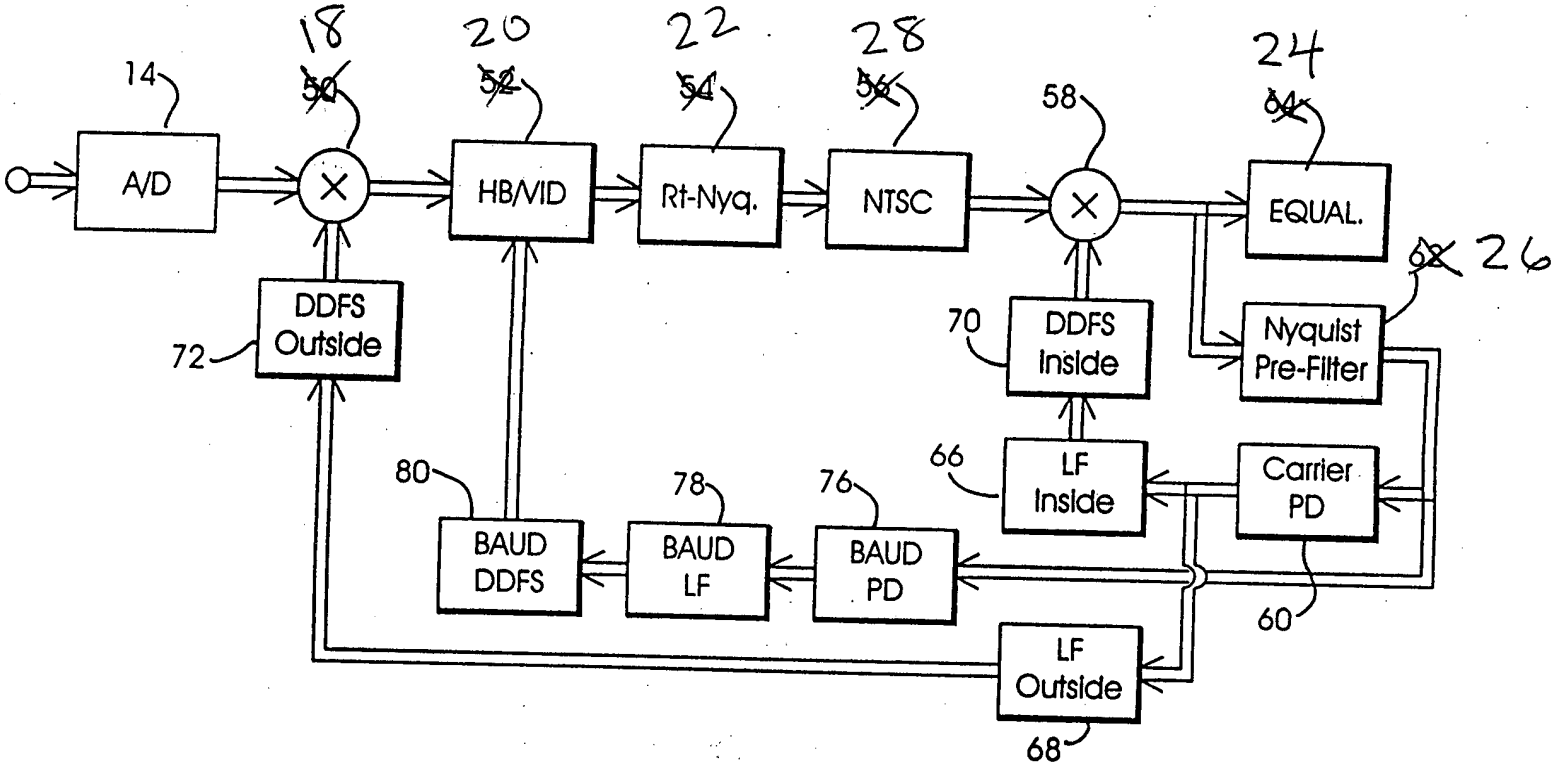
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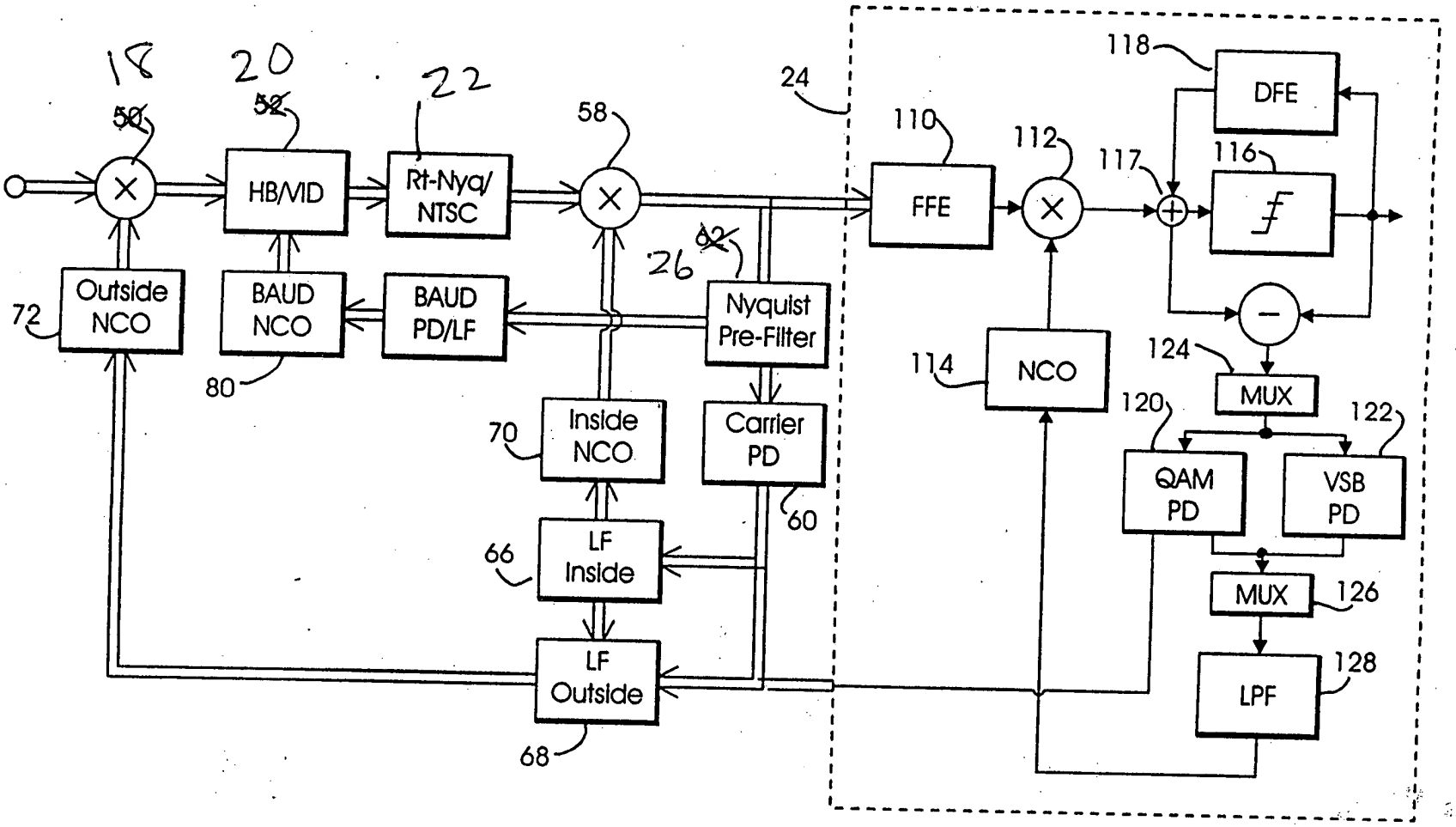
FIG. 4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72
BAUD
NCO
80
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Pre-Filter
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124
MUX
120
122
QAM
PD
VSB
PD
70
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PD
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66
LF
Inside
MUX
126
LF
Outside
68
LPF
128

FIG. 9